Smart 45nm Foundry CMOS with Mask-Lite™ Reduced Mask Costs

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Abstract: American Semiconductor has created Mask-Lite which is a layout and fabrication strategy that reduces mask costs and improves access to advanced 45nm bulk CMOS from their ITAR registered and TRUSTED ready on-shore commercial foundry.

Keywords: 45nm, CMOS, bulk CMOS, 1D layout, grated layout, Mask-Lite

Introduction

Advanced semiconductor fabrication technologies drive IC capabilities through increased performance and higher densities. However, these benefits come with a high financial cost driven by lithography equipment, complex mask fabrication, complicated design rules, and expensive EDA tools. This has a negative effect on many military and aerospace programs. The high cost of entry for 90nm process nodes and below often precludes products from being designed in advanced processes. Additionally, the high cost of entry for equipment limits the availability of advanced process nodes in on-shore facilities that can meet ITAR and TRUSTED requirements.

American Semiconductor's 45nm bulk CMOS dual use foundry process addresses these cost drivers with Mask-Lite technology, reducing mask costs up to 90% and providing affordable access to advanced semiconductor fabrication.

Mask-Lite™ Overview

Mask-Lite is an approach to layout and fabrication focused on simplifying masks, improving performance and reducing cost. One of the fundamentals of Mask-Lite is the use of one dimensional (1D) layout techniques, also known as unidirectional gridded layout (Figure 1). The Mask-Lite implementation of 1D layout uses a pattern of repeating lines for critical dimension layers such as poly and metal. These lines repeat at a fixed pitch across the wafer (Figure 2). Devices are formed by cutting the lines as desired in subsequent process steps as illustrated in Figure 3.

American Semiconductor's 45nm CMOS process, AS045BK, has been designed with Mask-Lite since its inception, providing both financial and technical benefits as detailed in the following sections. AS045BK with Mask-Lite is run using 193nm dry lithography, which is a proven industry standard approach to advanced CMOS technology.

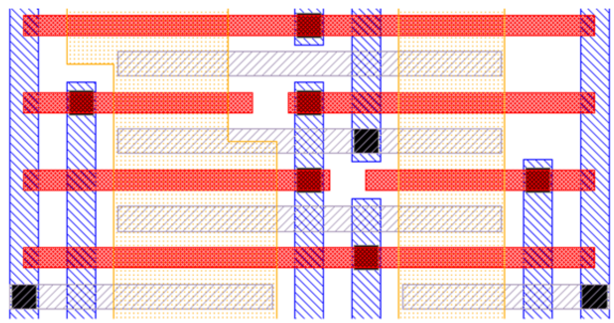

Figure 1. Mask-Lite 1D layout example

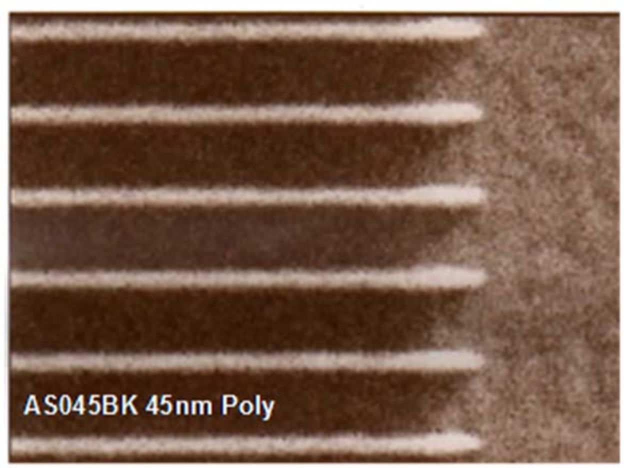

Figure 2. AS045BK 1D poly lines (photolithography)

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14. ABSTRACT

American Semiconductor has created Mask- Lite which is a layout and fabrication strategy that reduces mask costs and improves access to advanced 45nm bulk CMOS from their ITAR registered and TRUSTED ready on-shore commercial foundry.

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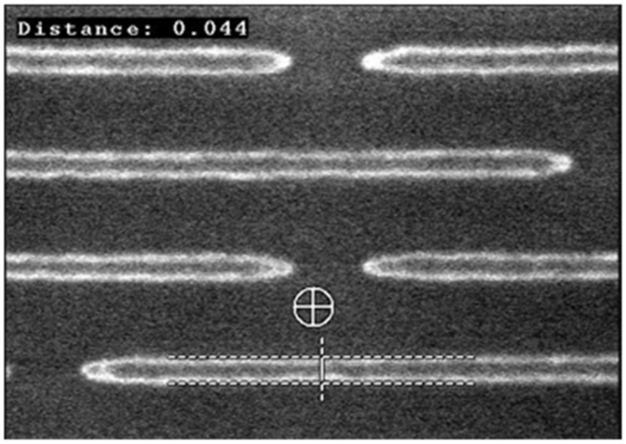

Figure 3. AS045BK 1D poly lines and cuts (photolithography)

Mask-Lite Reduced Mask Costs

One of the most significant costs for 45nm designs is the costs of the photomasks. Mask-Lite addresses this by reducing mask costs up to 90%, thereby dramatically reducing the direct costs of 45nm IC projects.

The most significant factor driving the costs of advanced photomasks is Optical Proximity Correction (OPC). The need for OPC is driven by the limitation of light to resolve fine detail onto the wafer. As shown in Figure 4, structures without OPC show irregularities such as rounded corners and line width shifts that may alter the characteristics or even functionality of fabricated devices.

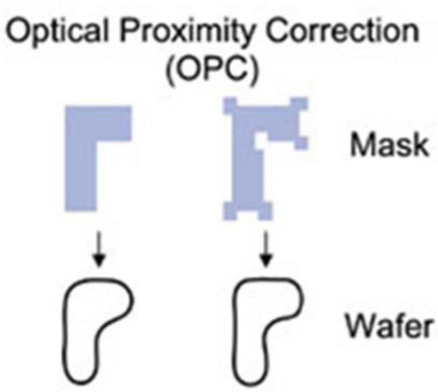

Figure 4. Drawn (top) versus printed (bottom) shapes without OPC (left) and with OPC (right).[1]

OPC mitigates these irregularities by adjusting the mask pattern such that the pattern on wafer more closely resembles the drawn feature as demonstrated in Figure 4. OPC mostly corrects line width differences based on density and line end shortening. The cost of OPC is due to building models for each process, applying the models to each mask layer, increased complexity for writing the masks, and increased write and inspection times.

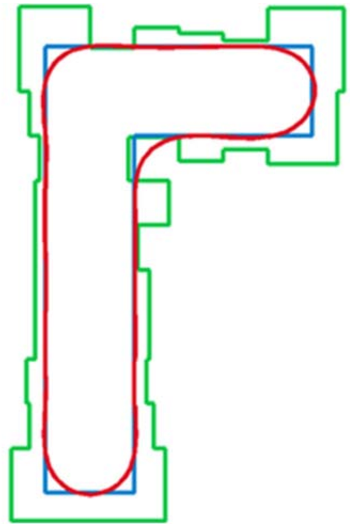

Figure 5. OPC example. The desired shape is in blue.
The shape after OPC is applied is in green.
The shape in red is how the shape prints on the wafer. [2]

Mask-Lite reduces or eliminates the need for OPC on 45nm masks. The 1D layout of fixed pitch lines does not require OPC to correct for density variances. Since there are no lines ends drawn, line end shortening is not a concern. By removing the features that drive OPC requirements, a major cost of 45nm mask fabrication is eliminated.

Additional mask cost savings are driven through the use of Multi Layer Reticles (MLRs). MLRs place mask layers of the same polarity and grade on the same physical reticle, reducing the number of reticles in the mask set. Up to 4 layers can be placed on the same reticle, reducing the reticle count up to 75%. The tradeoff for MLRs is the maximum field size available. For example, a Single Layer Reticle (SLR) mask set may have a maximum field size of 20mm x 20mm, where a MLR would reduce the maximum field size to 10mm x 10mm.

The cost reductions enabled through Mask-Lite are substantial. American Semiconductor delivers these cost reductions to customers for both dedicated and Multi-Project Wafer (MPW) runs. The availability of MPWs at a significantly reduced cost greatly increases the access to advanced 45nm CMOS technology.

Mask-Lite Simplifies Design Rules

As process nodes shrink, design rules become more numerous and complex. For example, moving to 90nm from 130nm increases the poly design rules by 47%, while further migration to 65nm increases the poly design rules another 65%. [3] The explosion in design rules increases the time it takes to design, layout, and verify in advanced nodes, resulting in higher cost.

Much of the increased design rule complexity is due to the poly layer, which is the most critical layer for control variation. Control of poly critical dimension is one of the most critical requirements in the process, due to the effect on transistor performance and variation.

Implementing Mask-Lite at 45nm provides predictable structures for poly and other critical layers such as M1 with reduced variation which simplifies design rules. By removing OPC requirements the design rules can be further simplified.

Designers do not face a steep learning curve or unfamiliar methodology to design with the Mask-Lite 1D layout. The AS045BK PDK contains a set of standard core cells that designers use just like any other set of core cells.

This results in a 45nm process with a greatly simplified design rule deck that saves significant time for design, layout, and verification, which translates into reduced project cost and improved time-to-market.

Area and Leakage Improvement

The most common concern for 1D layout is that it is perceived to increase area. However, in practice the opposite is true. Silicon results on 90nm, 65nm, and 45nm show area reductions of 20%. [4] This is achieved by layout techniques and optimizing the process technology for the fixed pitch and regular pattern of Mask-Lite.

Leakage is reduced by Mask-Lite's tight control of poly critical dimensions. Transistor off current varies exponentially with gate length. Consequently, any shortening of the gate length across the width of a transistor will increase leakage. By reducing the poly variability, drain-source leakage can be reduced by 47%. [4]

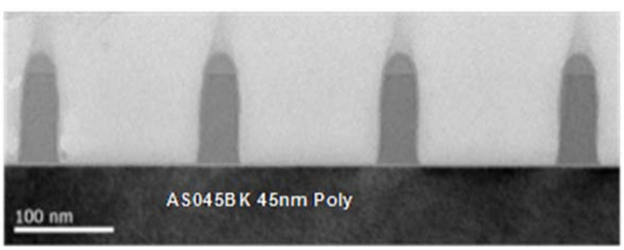

Figure 6. Cross-section of AS045BK 1D 45nm poly lines

Conclusions

As CMOS technology nodes shrink, the cost to access advanced geometries increases. Integrating Mask-Lite into their 45nm process allows American Semiconductor to address the cost drivers of advanced technology and deliver a leading edge process at a cost point viable for low volume requirements such as R&D, prototyping, and military/aerospace programs.

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